

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10007	"708"/\$.cls. and (multiplier\$1 or multiplication or multiplying) and @ad<"20030930"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:19
L2	750	1 and Booth\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:19
L3	574	2 and (encod\$5 or decod\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:10
L4	20	3 and (logic adj cell\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:15
L5	9	1 and ((BELLUOMINI.in. and WENDY.in.) or (NGO.in. and HUNG.in.) or (SAWADA.in. and JUN.in.))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:12
L6	6177	1 and ((multiplier\$1 or multiplication or multiplying).ti. or (multiplier\$1 or multiplication or multiplying).clm. or (multiplier\$1 or multiplication or multiplying).ab.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:19
L7	49168	6and Booth\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:19
L8	597	6 and Booth\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:19

EAST Search History

L9	162	8 and transistor\$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:20
L10	151	9 and (multiplex\$3 or select\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:20
L11	33	10 and (transistor\$1.ti. or transistor\$1.clm. or transistor\$1.ab.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:34
L12	2	"6173304".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:41
L13	15	9 and (PMOS or P-MOS or (P adj MOS))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/02 15:42
L14	14	("4472788" "5231636" "5553010" "5671166" "5751614" "5773995" "5781457" "5802556" "5809320" "5819056" "5991786").PN. OR ("6393446"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/02 15:47
L15	13	("4573137" "4575812" "4644488" "4813008" "4817029" "4887233" "5040139" "5146421" "5181184" "5231415" "5325321" "5343417" "5818743").PN. OR ("6393454"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/02 15:49
L16	15	("4965762" "4972362" "5150322" "5208489" "5208490" "5424734" "5524088" "5640108" "5668525" "5740094" "5748517" "5870322" "5935202").PN. OR ("6275841"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/02 15:50

□ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

SUPPORT

Results for "(belluomini w.<in>au)"

Your search matched 9 of 1450046 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

 e-mail  printer friendly

» Search Options

[View Session History](#)

[New Search](#)

Modify Search

(belluomini w.<in>au)

Search 

☐ Check to search only within this results set

Display Format: ☒ Citation ☐ Citation & Abstract

 **view selected items**

[Select All](#) [Deselect All](#)

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard



1. Timed state space exploration using POSETs

Belluomini, W.; Myers, C.J.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
Volume 19, Issue 5, May 2000 Page(s):501 - 520
Digital Object Identifier 10.1109/43.845076

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(488 KB\)](#) IEEE JNL
[Rights and Permissions](#)



2. Timed circuit verification using TEL structures

Belluomini, W.; Myers, C.J.; Hofstee, H.P.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
Volume 20, Issue 1, Jan. 2001 Page(s):129 - 146
Digital Object Identifier 10.1109/43.905681

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(384 KB\)](#) IEEE JNL
[Rights and Permissions](#)



3. An 8GHz floating-point multiply

Belluomini, W.; Jamsek, D.; Martin, A.; McDowell, C.; Montoye, R.; Nguyen, T.; Hung Ngo;
Sawada, J.; Vo, I.; Datta, R.;
[Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE](#)
[International](#)
6-10 Feb. 2005 Page(s):374 - 604 Vol. 1
Digital Object Identifier 10.1109/ISSCC.2005.1494025

[AbstractPlus](#) | [Full Text: PDF\(271 KB\)](#) | [Multimedia](#) IEEE CNF
[Rights and Permissions](#)



4. A low latency and low power dynamic Carry Save Adder

Datta, R.; Abraham, J.A.; Montoye, R.; Belluomini, W.; Hung Ngo; McDowell, C.; Kuang, J.B.;
Nowka, K.;
[Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on](#)
Volume 2, 23-26 May 2004 Page(s):II - 477-80 Vol.2

[AbstractPlus](#) | [Full Text: PDF\(375 KB\)](#) IEEE CNF
[Rights and Permissions](#)



5. A double precision floating point multiply

Montoye, R.; Belluomini, W.; Ngo, H.; McDowell, C.; Sawada, J.; Nguyen, T.; Veraa, B.;
Wagoner, J.; Lee, M.;
[Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE](#)
[International](#)
2003 Page(s):336 - 337 vol.1
Digital Object Identifier 10.1109/ISSCC.2003.1234323

[AbstractPlus](#) | [Full Text: PDF\(428 KB\)](#) | [Multimedia](#) IEEE CNF
[Rights and Permissions](#)

6. **Timed circuits: a new paradigm for high-speed design**
Myers, C.J.; Belluomini, W.; Killpack, K.; Mercer, E.; Peskin, E.; Hao Zheng;
Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001. Asia and South Pacific
30 Jan.-2 Feb. 2001 Page(s):335 - 340
Digital Object Identifier 10.1109/ASPDAC.2001.913329
[AbstractPlus](#) | Full Text: [PDF\(492 KB\)](#) IEEE CNF
[Rights and Permissions](#)
7. **Verification of delayed-reset domino circuits using ATACS**
Belluomini, W.; Myers, C.J.; Hofstee, H.P.;
Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings., Fifth International Symposium on
19-21 April 1999 Page(s):3 - 12
Digital Object Identifier 10.1109/ASYNC.1999.761518
[AbstractPlus](#) | Full Text: [PDF\(144 KB\)](#) IEEE CNF
[Rights and Permissions](#)
8. **Timed circuit synthesis using implicit methods**
Thacker, R.A.; Belluomini, W.; Myers, C.J.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):181 - 188
Digital Object Identifier 10.1109/ICVD.1999.745146
[AbstractPlus](#) | Full Text: [PDF\(180 KB\)](#) IEEE CNF
[Rights and Permissions](#)
9. **Efficient timing analysis algorithms for timed state space exploration**
Belluomini, W.; Myers, C.J.;
Advanced Research in Asynchronous Circuits and Systems, 1997. Proceedings., Third International Symposium on
7-10 April 1997 Page(s):88 - 100
Digital Object Identifier 10.1109/ASYNC.1997.587166
[AbstractPlus](#) | Full Text: [PDF\(1300 KB\)](#) IEEE CNF
[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2006 IEEE – All Rights Reserved

Indexed by
 **Inspection**

☐ Author Search

[BROWSE](#)

[SEARCH](#)

[IEEE XPLORE GUIDE](#)

[SUPPORT](#)



OPTION 1

Quick Find an Author:

Enter a name to locate articles written by that author.



Select a name to view articles written by that author

Belluomini W.

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.



OPTION 2

Browse alphabetically

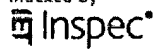
Select a letter from the list.

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2006 IEEE – All Rights Reserved

Indexed by



Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

SUPPORT

Results for "(sawada j.<in>au)"

Your search matched 20 of 1450046 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

 e-mail  printer friendly


» Search Options

[View Session History](#)

[New Search](#)

Modify Search:

(sawada j.<in>au)

Search 

☐ Check to search only within this results set

Display Format: ☒ Citation ☐ Citation & Abstract

» Key


IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

 **view selected items**

[Select All](#) [Deselect All](#)

- ☐ **1. A dynamic power system model for teaching and research**
Yao-nan Yu; Sawada, J.H.; Wvong, M.D.;
[Power Apparatus and Systems, IEEE Transactions on](#)
Volume 95, Issue 4, Part 1, July 1976 Page(s):1507 - 1514
[AbstractPlus](#) | Full Text: [PDF\(792 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **2. Appropriate HVDC transmission simulation models for various power system stability studies**
Arabi, S.; Kundur, P.; Sawada, J.H.;
[Power Systems, IEEE Transactions on](#)
Volume 13, Issue 4, Nov. 1998 Page(s):1292 - 1297
Digital Object Identifier 10.1109/59.736267
[AbstractPlus](#) | Full Text: [PDF\(588 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **3. Harmonic impedance measurement using three-phase transients**
Nagpal, M.; Xu, W.; Sawada, J.;
[Power Delivery, IEEE Transactions on](#)
Volume 13, Issue 1, Jan. 1998 Page(s):272 - 277
Digital Object Identifier 10.1109/61.660889
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(632 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **4. Controlled closing on shunt reactor compensated transmission lines. II. Application of closing control device for high-speed autoreclosing on BC Hydro 500 kV transmission line**
Froehlich, K.; Hoelzl, C.; Stanek, M.; Carvalho, A.C.; Hofbauer, W.; Hoegg, P.; Avent, B.L.; Peelo, D.F.; Sawada, J.H.;
[Power Delivery, IEEE Transactions on](#)
Volume 12, Issue 2, April 1997 Page(s):741 - 746
Digital Object Identifier 10.1109/61.584360
[AbstractPlus](#) | Full Text: [PDF\(572 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **5. Controlled closing on shunt reactor compensated transmission lines. I. Closing control device development**
Froehlich, K.; Hoelzl, C.; Stanek, M.; Carvalho, A.C.; Hofbauer, W.; Hoegg, P.; Avent, B.L.; Peelo, D.F.; Sawada, J.H.;
[Power Delivery, IEEE Transactions on](#)
Volume 12, Issue 2, April 1997 Page(s):734 - 740
Digital Object Identifier 10.1109/61.584359
[AbstractPlus](#) | Full Text: [PDF\(672 KB\)](#) IEEE JNL

6. **Mitigation of circuit breaker transient recovery voltages associated with current limiting reactors**
Peelo, D.F.; Polovick, G.S.; Sawada, J.H.; Diamanti, P.; Presta, R.; Sarshar, A.; Beauchemin, R.;
Power Delivery, IEEE Transactions on
Volume 11, Issue 2, April 1996 Page(s):865 - 871
Digital Object Identifier 10.1109/61.489345
AbstractPlus | Full Text: PDF(462 KB) IEEE JNL
Rights and Permissions
7. **Experimental evaluation of a UHV tower model for lightning surge analysis**
Yamada, T.; Mochizuki, A.; Sawada, J.; Zaima, E.; Kawamura, T.; Ametani, A.; Ishii, M.; Kato, S.;
Power Delivery, IEEE Transactions on
Volume 10, Issue 1, Jan. 1995 Page(s):393 - 402
Digital Object Identifier 10.1109/61.368374
AbstractPlus | Full Text: PDF(808 KB) IEEE JNL
Rights and Permissions
8. **Harmonics from SVC transformer saturation with direct current offset**
Xu, W.; Martinich, T.G.; Sawada, J.H.; Mansour, Y.;
Power Delivery, IEEE Transactions on
Volume 9, Issue 3, July 1994 Page(s):1502 - 1509
Digital Object Identifier 10.1109/61.311218
AbstractPlus | Full Text: PDF(660 KB) IEEE JNL
Rights and Permissions
9. **Development of suspension-type arresters for transmission lines**
Yamada, T.; Sawada, J.; Zaima, E.; Irie, T.; Ohashi, T.; Yoshida, S.; Kawamura, T.;
Power Delivery, IEEE Transactions on
Volume 8, Issue 3, July 1993 Page(s):1052 - 1060
Digital Object Identifier 10.1109/61.252631
AbstractPlus | Full Text: PDF(652 KB) IEEE JNL
Rights and Permissions
10. **A Mobile Robot for Inspection of Power Transmission Lines**
Sawada, J.; Kusumoto, K.; Munakata, T.; Maikawa, Y.; Ishikawa, Y.;
Power Engineering Review, IEEE
Volume 11, Issue 1, January 1991 Page(s):57
Digital Object Identifier 10.1109/MPER.1991.88671
AbstractPlus | Full Text: PDF(264 KB) IEEE JNL
Rights and Permissions
11. **A mobile robot for inspection of power transmission lines**
Sawada, J.; Kusumoto, K.; Maikawa, Y.; Munakata, T.; Ishikawa, Y.;
Power Delivery, IEEE Transactions on
Volume 6, Issue 1, Jan. 1991 Page(s):309 - 315
Digital Object Identifier 10.1109/61.103753
AbstractPlus | Full Text: PDF(608 KB) IEEE JNL
Rights and Permissions
12. **Verifying the FM9801 microarchitecture**
Hunt, W.A., Jr.; Sawada, J.;
Micro, IEEE
Volume 19, Issue 3, May-June 1999 Page(s):47 - 55
Digital Object Identifier 10.1109/40.768503
AbstractPlus | References | Full Text: PDF(1380 KB) IEEE JNL
Rights and Permissions
13. **Frequency-dependent impedance of vertical conductors and a multiconductor tower model**
Ametani, A.; Kasai, Y.; Sawada, J.; Mochizuki, A.; Yamada, T.;

14. BC Hydro harmonic resonance experience

Gin, S.B.; Sawada, J.H.; Treasure, T.R.;
[Power Engineering Society Summer Meeting, 2000. IEEE](#)
Volume 2, 16-20 July 2000 Page(s):1088 - 1093 vol. 2
Digital Object Identifier 10.1109/PESS.2000.867529

[AbstractPlus](#) | Full Text: [PDF\(468 KB\)](#) IEEE CNF
[Rights and Permissions](#)

15. An 8GHz floating-point multiply

Belluomini, W.; Jamsek, D.; Martin, A.; McDowell, C.; Montoye, R.; Nguyen, T.; Hung Ngo;
Sawada, J.; Vo, I.; Datta, R.;
[Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE](#)
[International](#)
6-10 Feb. 2005 Page(s):374 - 604 Vol. 1
Digital Object Identifier 10.1109/ISSCC.2005.1494025

[AbstractPlus](#) | Full Text: [PDF\(271 KB\)](#) | [Multimedia](#) IEEE CNF
[Rights and Permissions](#)

16. Modeling and control of elastic plates and cylindrical shell

Ohsumi, A.; Inomata, T.; Sawada, J.;
[SICE 2003 Annual Conference](#)
Volume 1, 2003 Page(s):545 - 550 Vol.1

[AbstractPlus](#) | Full Text: [PDF\(344 KB\)](#) IEEE CNF
[Rights and Permissions](#)

17. A double precision floating point multiply

Montoye, R.; Belluomini, W.; Ngo, H.; McDowell, C.; Sawada, J.; Nguyen, T.; Veraa, B.;
Wagoner, J.; Lee, M.;
[Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE](#)
[International](#)
2003 Page(s):336 - 337 vol.1
Digital Object Identifier 10.1109/ISSCC.2003.1234323

[AbstractPlus](#) | Full Text: [PDF\(428 KB\)](#) | [Multimedia](#) IEEE CNF
[Rights and Permissions](#)

18. Development of a proton accelerator for the JAERI Neutron Science Project

Akaoka, N.; Chishiro, E.; Hasegawa, K.; Ichihara, M.; Ikegami, M.; Ito, T.; Kinsho, M.; Kusano,
J.; Minehara, E.; Mizumoto, M.; Mukugi, K.; Noda, F.; Oguri, H.; Ouchi, N.; Sawada, J.; Takado,
H.; Takeda, O.; Tomisawa, T.; Yokomizo, H.;
[Particle Accelerator Conference, 1999. Proceedings of the 1999](#)
Volume 5, 27 March-2 April 1999 Page(s):3546 - 3548 vol.5
Digital Object Identifier 10.1109/PAC.1999.792365

[AbstractPlus](#) | Full Text: [PDF\(188 KB\)](#) IEEE CNF
[Rights and Permissions](#)

19. A wafer scale fail bit analysis system for VLSI memory yield improvement

Sakai, Y.; Sawada, J.; Sakamoto, W.; Murato, J.; Kawamoto, H.; Sakai, K.; Nakamuta, K.;
[Microelectronic Test Structures, 1990. ICMTS 1990. Proceedings of the 1990 International](#)
[Conference on](#)
5-7 March 1990 Page(s):175 - 178
Digital Object Identifier 10.1109/ICMTS.1990.67899

[AbstractPlus](#) | Full Text: [PDF\(164 KB\)](#) IEEE CNF
[Rights and Permissions](#)

20. Control of line impedance and phase-shifter and its analysis with a machine flux based simulation program

Iyoda, I.; Kono, Y.; Suzuki, H.; Sawada, J.; Matoba, S.;
[Advances in Power System Control, Operation and Management, 1991. APSCOM-91., 1991](#)
[International Conference on](#)
5-8 Nov 1991 Page(s):668 - 673 vol.2



[Author Search](#)

[BROWSE](#)

[SEARCH](#)

[IEEE XPLORE GUIDE](#)

[SUPPORT](#)



OPTION 1

Quick Find an Author:

Enter a name to locate articles written by that author.



Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.



OPTION 2

Browse alphabetically

Select a letter from the list.

[A](#) [B](#) [C](#) [D](#) [E](#) [F](#) [G](#) [H](#) [I](#) [J](#) [K](#) [L](#) [M](#) [N](#) [O](#) [P](#) [Q](#) [R](#) [S](#) [T](#) [U](#) [V](#) [W](#) [X](#) [Y](#) [Z](#)

Select a name to view articles written by that author

[Sawada A.](#)

[Sawada G.](#)

[Sawada I.](#)

[Sawada K.](#)

[Sawada R.](#)

[Sawada Y.](#)

[Sawada C.](#)

[Sawada H.](#)

[Sawada J.](#)

[Sawada M.](#)

[Sawada S.](#)

[Sawadaishi T.](#)

[Sawada F.](#)

[Sawada Hiroshi](#)

[Sawada J. H.](#)

[Sawada N.](#)

[Sawada T.](#)

□ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

SUPPORT

Results for "(ngo h. c.<in>au)"

Your search matched 6 of 1450046 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

e-mail printer friendly

» Search Options

[View Session History](#)

[New Search](#)

Modify Search

(ngo h. c.<in>au)

Search

☐ Check to search only within this results set

Display Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

view selected items [Select All](#) [Deselect All](#)

- ☐ 1. **A 32-bit PowerPC system-on-a-chip with support for dynamic voltage scaling and dynamic frequency scaling**
Nowka, K.J.; Carpenter, G.D.; MacDonald, E.W.; Ngo, H.C.; Brock, B.C.; Ishii, K.I.; Nguyen, T.Y.; Burns, J.L.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 37, Issue 11, Nov. 2002 Page(s):1441 - 1447
Digital Object Identifier 10.1109/JSSC.2002.803941
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(494 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. **A low-overhead virtual rail technique for SRAM leakage power reduction**
Kuang, J.B.; Ngo, H.C.; Nowka, K.J.; Law, J.C.; Joshi, R.V.;
[Computer Design: VLSI in Computers and Processors, 2005. ICCD 2005. Proceedings. 2005 IEEE International Conference on](#)
2-5 Oct. 2005 Page(s):574 - 579
Digital Object Identifier 10.1109/ICCD.2005.11
[AbstractPlus](#) | Full Text: [PDF\(256 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 3. **Wide limited switch dynamic logic circuit implementations**
Sivagnaname, J.; Ngo, H.C.; Nowka, K.J.; Montoye, R.K.; Brown, R.B.;
[VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on](#)
3-7 Jan. 2006 Page(s):6 pp.
Digital Object Identifier 10.1109/VLSID.2006.171
[AbstractPlus](#) | Full Text: [PDF\(456 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 4. **Dynamic circuit techniques using independently controlled double-gate devices**
Kuang, J.B.; Kim, K.; Chuang, C.T.; Ngo, H.C.; Nowka, K.J.;
[SOI Conference, 2005. Proceedings. 2005 IEEE International](#)
3-6 Oct. 2005 Page(s):74 - 76
Digital Object Identifier 10.1109/SOI.2005.1563539
[AbstractPlus](#) | Full Text: [PDF\(1680 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 5. **Controlled-load limited switch dynamic logic circuit**
Sivagnaname, J.; Ngo, H.C.; Nowka, K.J.; Montoye, R.K.; Brown, R.B.;
[Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on](#)
21-23 March 2005 Page(s):83 - 87
Digital Object Identifier 10.1109/ISQED.2005.35
[AbstractPlus](#) | Full Text: [PDF\(192 KB\)](#) IEEE CNF
[Rights and Permissions](#)

6. 470 ps 64-bit parallel binary adder [for CPU chip]

Jaehong Park; Ngo, H.C.; Silberman, J.A.; Dhong, S.H.;

VLSI Circuits, 2000. Digest of Technical Papers. 2000 Symposium on
15-17 June 2000 Page(s): 192 - 193

Digital Object Identifier 10.1109/VLSIC.2000.852887

AbstractPlus | Full Text: PDF(172 KB) IEEE CNF
Rights and Permissions

[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2006 IEEE – All Rights Reserved

Indexed by
 Inspec®

☐ Author Search

[BROWSE](#)

[SEARCH](#)

[IEEE XPLORE GUIDE](#)

[SUPPORT](#)

Select a name to view articles written by that author



OPTION 1

Quick Find an Author:

Enter a name to locate articles written by that author.

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.



OPTION 2

Browse alphabetically

Select a letter from the list.

[A](#) [B](#) [C](#) [D](#) [E](#) [F](#) [G](#) [H](#) [I](#) [J](#) [K](#) [L](#) [M](#) [N](#) [O](#) [P](#) [Q](#) [R](#) [S](#) [T](#) [U](#) [V](#) [W](#) [X](#) [Y](#) [Z](#)

[Ngo A. D.](#)

[Ngo C.](#)

[Ngo C. W.](#)

[Ngo D.](#)

[Ngo D. C. L.](#)

[Ngo E.](#)

[Ngo G.](#)

[Ngo H. D.](#)

[Ngo H. T.](#)

[Ngo Hoc](#)

[Ngo K.](#)

[Ngo K. D.](#)

[Ngo L.](#)

[Ngo M.](#)

[Ngo M. N.](#)

[Ngo N.](#)

[Ngo P.](#)

[Ngo A. T.](#)

[Ngo C. L. D.](#)

[Ngo C. Y.](#)

[Ngo D. B. L.](#)

[Ngo D. M.](#)

[Ngo F.](#)

[Ngo H.](#)

[Ngo H. H.](#)

[Ngo H. X.](#)

[Ngo J.](#)

[Ngo K. B.](#)

[Ngo K. D. T.](#)

[Ngo L. T.](#)

[Ngo M. -L. D.](#)

[Ngo M. T.](#)

[Ngo N. H.](#)

[Ngo P. D. -T.](#)

[Ngo B.](#)

[Ngo C. M.](#)

[Ngo Chon Chet](#)

[Ngo D. C.](#)

[Ngo Duong Sinh](#)

[Ngo F. C.](#)

[Ngo H. C.](#)

[Ngo H. Q.](#)

[Ngo Hai Dong](#)

[Ngo J. C.](#)

[Ngo K. C. T.](#)

[Ngo K. T.](#)

[Ngo L. V.](#)

[Ngo M. -V.](#)

[Ngo M. V.](#)

[Ngo N. Q.](#)

Inventor Information for 10/675674

Inventor Name	City	State/Country
BELLUOMINI, WENDY ANN	AUSTIN	TEXAS
NGO, HUNG CAI	AUSTIN	TEXAS
SAWADA, JUN	AUSTIN	TEXAS

[Appln Info](#)[Contents](#)[Petition Info](#)[Atty/Agent Info](#)[Continuity/Reexam .](#)[Foreign Data](#)[Invento](#)

Search Another: Application#

or Patent#

PCT /

/

or PG PUBS #

Attorney Docket #

Bar Code #

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Inventor Name Search Result

Your Search was:

Last Name = BELLUOMINI

First Name = WENDY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09344653	Not Issued	161	06/25/1999	METHODOLOGY AND APPARATUS FOR HTE DESIGN, ANALYSIS, AND VERIFICATION OF TIMED CIRCUITS	BELLUOMINI, WENDY
10242214	6690204	150	09/12/2002	LIMITED SWITCH DYNAMIC LOGIC CIRCUIT	BELLUOMINI, WENDY A.
10242236	6873188	150	09/12/2002	LIMITED SWITCH DYNAMIC LOGIC SELECTOR CIRCUITS	BELLUOMINI, WENDY A.
10702989	Not Issued	41	11/06/2003	4-to-2 carry save adder using limited switching dynamic logic	BELLUOMINI, WENDY A.
10702992	Not Issued	90	11/06/2003	COMPUTING CARRY-IN BIT TO MOST SIGNIFICANT BIT CARRY SAVE ADDER IN CURRENT STAGE	BELLUOMINI, WENDY A.
09891343	Not Issued	168	06/26/2001	Method and system for managing innovation by encouraging reusability and subsequent reuse of design components	BELLUOMINI, WENDY ANN
10116612	6650145	150	04/04/2002	CIRCUITS AND SYSTEMS FOR LIMITED SWITCH DYNAMIC LOGIC	BELLUOMINI, WENDY ANN
10322074	6731129	150	12/17/2002	APPARATUS FOR MEASURING CAPACITANCE OF A SEMICONDUCTOR DEVICE	BELLUOMINI, WENDY ANN
10388977	6891399	150	03/13/2003	VARIABLE PULSE WIDTH AND PULSE SEPARATION CLOCK GENERATOR	BELLUOMINI, WENDY ANN
10670832	7047468	150	09/25/2003	METHOD AND APPARATUS FOR LOW OVERHEAD CIRCUIT SCAN	BELLUOMINI, WENDY ANN
10675674	Not Issued	71	09/30/2003	Fused booth encoder multiplexer	BELLUOMINI, WENDY ANN
10793460	7046094	150	03/04/2004	METHOD AND RING OSCILLATOR CIRCUIT FOR MEASURING CIRCUIT DELAYS OVER A WIDE OPERATING RANGE	BELLUOMINI, WENDY ANN
11168691	Not Issued	30	06/28/2005	Method and apparatus for power consumption reduction in a limited-switch dynamic logic (LSDL) circuit	BELLUOMINI, WENDY ANN
11168718	Not Issued	30	06/28/2005	Dynamic logical circuit having a pre-charge element separately controlled by a voltage-asymmetric clock	BELLUOMINI, WENDY ANN

Inventor Search Completed: No Records to Display.

	Last Name	First Name	
Search Another: Inventor	BELLUOMINI	WENDY	<input type="button" value="Search"/>

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Inventor Name Search Result

Your Search was:

Last Name = NGO

First Name = HUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09731140	Not Issued	161	12/06/2000	On-line management of product delivery	NGO, HUNG
11219100	Not Issued	25	09/01/2005	System for and method of emulating electronic input devices	NGO, HUNG
60172361	Not Issued	159	12/16/1999	On-line management of product delivery	NGO, HUNG
09649446	6675182	150	08/25/2000	METHOD AND APPARATUS FOR PERFORMING ROTATE OPERATIONS USING CASCADED MULTIPLEXERS	NGO, HUNG C.
09918809	6963629	150	07/31/2001	ADAPTIVE PHASE LOCKED LOOP	NGO, HUNG C.
09974969	6809602	150	10/11/2001	MULTI-MODE VCO	NGO, HUNG C.
09974985	6515530	150	10/11/2001	DYNAMICALLY SCALABLE LOW VOLTAGE CLOCK GENERATION SYSTEM	NGO, HUNG C.
09974987	6483888	150	10/11/2001	CLOCK DIVIDER WITH BYPASS AND STOP CLOCK	NGO, HUNG C.
09974990	6501304	150	10/11/2001	GLITCH-LESS CLOCK SELECTOR	NGO, HUNG C.
09975187	6529082	150	10/11/2001	DUAL MODE CHARGE PUMP	NGO, HUNG C.
10242214	6690204	150	09/12/2002	LIMITED SWITCH DYNAMIC LOGIC CIRCUIT	NGO, HUNG C.
10242236	6873188	150	09/12/2002	LIMITED SWITCH DYNAMIC LOGIC SELECTOR CIRCUITS	NGO, HUNG C.
10655375	6960939	150	09/04/2003	LIMITED SWITCH DYNAMIC LOGIC CIRCUIT WITH KEEPER	NGO, HUNG C.
10702989	Not Issued	41	11/06/2003	4-to-2 carry save adder using limited switching dynamic logic	NGO, HUNG C.
10702992	Not Issued	90	11/06/2003	COMPUTING CARRY-IN BIT TO MOST SIGNIFICANT BIT CARRY SAVE ADDER IN CURRENT STAGE	NGO, HUNG C.
10718062	6963250	150	11/20/2003	VOLTAGE CONTROLLED OSCILLATOR WITH SELECTABLE FREQUENCY RANGES	NGO, HUNG C.

10718063	6956793	150	11/20/2003	PHASE CLOCK SELECTOR FOR GENERATING A NON-INTEG FREQUENCY DIVISION	NGO, HUNG C.
10733936	6940312	150	12/11/2003	LOW SWITCHING POWER LIMITED SWITCH DYNAMIC LOGIC	NGO, HUNG C.
10733950	6919739	150	12/11/2003	FEEDFORWARD LIMITED SWITCH DYNAMIC LOGIC CIRCUIT	NGO, HUNG C.
10763093	7002420	150	01/22/2004	INTERLEAVED VCO WITH BODY VOLTAGE FREQUENCY RANGE CONTROL	NGO, HUNG C.
10821047	7046063	150	04/08/2004	INTERFACE CIRCUIT FOR COUPLING BETWEEN LOGIC CIRCUIT DOMAINS	NGO, HUNG C.
10821048	6975134	150	04/08/2004	BUFFER/DRIVER CIRCUITS	NGO, HUNG C.
10835501	6980018	150	04/29/2004	SELF LIMITING GATE LEAKAGE DRIVER	NGO, HUNG C.
10840708	6872991	150	05/06/2004	LOW GATE-LEAKAGE VIRTUAL RAIL CIRCUIT	NGO, HUNG C.
10916980	7061265	150	08/12/2004	CIRCUIT FOR CONTROLLING LEAKAGE	NGO, HUNG C.
10926597	Not Issued	25	08/26/2004	Power-gating cell for virtual power rail control	NGO, HUNG C.
10942419	Not Issued	41	09/16/2004	Dynamic leakage control circuit	NGO, HUNG C.
10960608	7057432	150	10/07/2004	LOW POWER HIGH FREQUENCY PHASE DETECTOR	NGO, HUNG C.
10988454	Not Issued	71	11/12/2004	Digital duty cycle corrector	NGO, HUNG C.
11034556	Not Issued	30	01/13/2005	Dynamic power and clock-gating method and circuitry	NGO, HUNG C.
11082805	7129754	150	03/17/2005	CONTROLLED LOAD LIMITED SWITCH DYNAMIC LOGIC CIRCUITRY	NGO, HUNG C.
11204401	Not Issued	30	08/16/2005	Dual-gate dynamic logic circuit with pre-charge keeper	NGO, HUNG C.
11211954	Not Issued	30	08/25/2005	Control circuitry for power gating virtual power supply rails at differing voltage potentials	NGO, HUNG C.
11260563	Not Issued	41	10/27/2005	Method and apparatus for fail-safe and restartable system clock generation	NGO, HUNG C.
11260571	Not Issued	30	10/27/2005	Cascaded pass-gate test circuit with interposed split-output drive devices	NGO, HUNG C.
11552158	Not Issued	25	10/24/2006	Test Structure for Characterizing Multi-Port Static Random Access Memory and Register File Arrays	NGO, HUNG C.
11553014	Not Issued	20	10/26/2006	PULSED LOCAL CLOCK BUFFER (LCB) CHARACTERIZATION RING	NGO, HUNG C.

				OSCILLATOR	
11554666	Not Issued	20	10/31/2006	Programmable Local Clock Buffer	NGO, HUNG C.
11554685	Not Issued	25	10/31/2006	Scannable Dynamic Logic Latch Circuit	NGO, HUNG C.
11559436	Not Issued	25	11/14/2006	Circuit Timing Monitor Having A Selectable-Path Ring Oscillator	NGO, HUNG C.
11560440	Not Issued	25	11/16/2006	Hybrid Keeper Circuit for Dynamic Logic	NGO, HUNG C.
11567395	Not Issued	19	01/01/0001	PARTIAL DATA FLOW FUNCTIONAL GATING USING STRUCTURAL OR PARTIAL OPERAND VALUE INFORMATION	NGO, HUNG C.
11608907	Not Issued	19	12/11/2006	System and Method for Implementing Simplified Arithmetic Logic Unit Processing of Value-Based Control Dependence Sequences	NGO, HUNG C.
08001372	5375223	150	01/07/1993	SINGLE REGISTER ARBITER CIRCUIT	NGO, HUNG C.
08461676	5742535	250	06/05/1995	PARALLEL CALCULATION OF EXPONENT AND STICKY BIT DURING NORMALIZATION	NGO, HUNG C.
08473308	5627774	150	06/07/1995	PARALLEL CALCULATION OF EXPONENT AND STICKY BIT DURING NORMALIZATION	NGO, HUNG C.
08478416	5742536	250	06/07/1995	PARALLEL CALCULATION OF EXPONENT AND STICKY BIT DURING NORMALIZATION	NGO, HUNG C.
08900261	5881274	150	07/25/1997	METHOD AND APPARATUS FOR PERFORMING ADD AND ROTATE AS A SINGLE INSTRUCTION WITHIN A PROCESSOR	NGO, HUNG C.
09523717	Not Issued	160	03/13/2000	Method and apparatus for implementing logic mask-programmable dynamic logic gates	NGO, HUNG CAI
09524901	6819141	150	03/14/2000	HIGH SPEED, STATIC DIGITAL MULTIPLEXER	NGO, HUNG CAI

[Search and Display More Records.](#)

Search Another: Inventor
Last Name
First Name

NGO
HUNG

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Inventor Name Search Result

Your Search was:

Last Name = SAWADA

First Name = JUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07545656	5103739	150	06/29/1990	APPARATUS FOR TRACKING AN OVERHEAD LINE AND AUTOMATICALLY MOVING AROUND OBSTACLES ON THE LINE	SAWADA, JUN
07794141	5281768	250	11/19/1991	SUSPENSION-TYPE LINE ARRESTER	SAWADA, JUN
09649446	6675182	150	08/25/2000	METHOD AND APPARATUS FOR PERFORMING ROTATE OPERATIONS USING CASCADED MULTIPLEXERS	SAWADA, JUN
10015224	Not Issued	168	12/13/2001	Hardware validation through binary decision diagrams including functions and equalities	SAWADA, JUN
10675674	Not Issued	71	09/30/2003	Fused booth encoder multiplexer	SAWADA, JUN
10829571	Not Issued	25	04/22/2004	Replaceable sequenced one-time pads for detection of cloned service client	SAWADA, JUN
10896505	Not Issued	71	07/22/2004	Scanning latches using selecting array	SAWADA, JUN
11315268	Not Issued	41	12/23/2005	Pressure distribution measurement system	SAWADA, JUN
10497114	7050007	150	09/24/2004	ELECTRONIC DEVICE WITH COMMUNICATION CAPABILITY	SAWADA, JUNICHI
10569917	Not Issued	30	02/28/2006	Ic card and method for producing the same	SAWADA, JUNICHI
10856653	Not Issued	30	05/28/2004	Method and apparatus for setting master node of ring network	SAWADA, JUNICHI
10857466	Not Issued	30	05/28/2004	Information provision system, terminal unit and relay unit forming part of that system, and image display customizing system	SAWADA, JUNICHI
10944915	Not Issued	93	09/21/2004	RELAYING APPARATUS AND COMMUNICATION SYSTEM	SAWADA, JUNICHI
11042786	Not Issued	30	01/25/2005	Portable type information processing terminal device	SAWADA, JUNICHI
11054556	Not Issued	30	02/10/2005	QoS control method, transmission apparatus and storage medium	SAWADA, JUNICHI
11060507	Not Issued	30	02/18/2005	Transmission device	SAWADA, JUNICHI

11067985	Not Issued	30	03/01/2005	Apparatus for preventing corrosion of contact	SAWADA, JUNICHI
11067986	Not Issued	25	03/01/2005	Circuit for preventing corrosion of contact	SAWADA, JUNICHI
11068393	Not Issued	30	03/01/2005	Method and apparatus for preventing corrosion of contact	SAWADA, JUNICHI
11101463	Not Issued	30	04/08/2005	Wireless repeater, the method for wireless repeating, and data communications system	SAWADA, JUNICHI
11340840	Not Issued	30	01/27/2006	Method and apparatus for multiplexing and demultiplexing data, and computer product	SAWADA, JUNICHI
11343289	Not Issued	30	01/31/2006	Data transmission apparatus for traffic control to maintain quality of service	SAWADA, JUNICHI
11384352	Not Issued	20	03/21/2006	Stolen vehicle recovery support apparatus	SAWADA, JUNICHI
11598753	Not Issued	19	11/14/2006	Driving information recoding apparatus	SAWADA, JUNICHI
11598756	Not Issued	19	11/14/2006	Driving information analysis apparatus and driving information analysis system	SAWADA, JUNICHI
11600191	Not Issued	20	11/16/2006	Apparatus, method, and computer product for discriminating object	SAWADA, JUNICHI
11601629	Not Issued	20	11/20/2006	Communication apparatus, communication control method, and computer product	SAWADA, JUNICHI

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name
 SAWADA

First Name
 JUN

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)